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I3DS SENSOR SUITE FOR SPACE ROBOTICS

Kristoffer Nyborg Gregertsen, PhD

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About me

- SINTEF Digital – Department of Mathematics and Cybernetics
- Research manager for automation and real-time systems
- PhD in cybernetics from NTNU on real-time system support in Ada with execution time for interrupts
- **We are hiring research scientist!**

SINTEF

SINTEF is one of Europe's largest independent research organisations

2000
Employees

75
Nationalities

4000
Customers

NOK 3.1 billion
Revenues

NOK 450 MILL
International sales

I3DS project

- Space Robotics Cluster (H2020)
  - Future robotics platform for ESA
  - Led by the PERASPERA project
  - 6 Operational Grants (OG's)
- I3DS – Integrated 3D Sensors
  - Thales Alenia Space is coordinator
  - SINTEF leads software development, integration and interface definition

ThalesAlenia Space
A Thales / Finmeccanica Company

SINTEF

Cranfield UNIVERSITY

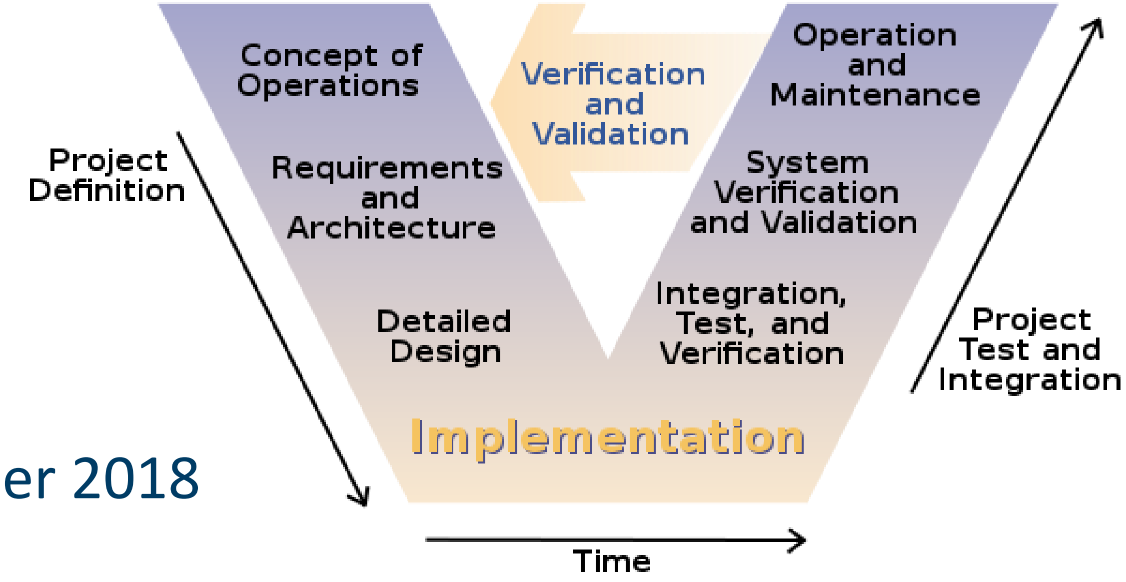
TERMA

PIAP

cosine

HERTZ SYSTEMS

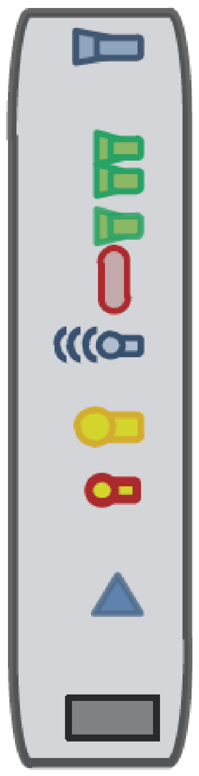
Project status



- Project phases defined as for ESA projects
- Kick-off in November 2016, finish November 2018
  - SRR in February 2017
  - PDR in July 2017
  - CDR in February 2018
- Now finishing integration phase of project lead by SINTEF
- Validation of sensor suite in demonstrators from July 2018
- Full integration with other OG's in next SRC calls, proposal submitted!

Project motivation and goal

- Develop and demonstrate a modular sensor suite for space robotics
  - Tight cooperation with OG's for middleware, autonomy and sensor fusion
  - TASTE framework with AADL and ASN.1 messages for system integration
  - Sensors, Instrument Control Unit (ICU) and software at **TRL5**
- Motivation: Reduce development time of space missions
  - Abstract away device specific details with standard interface for sensor class
  - Allows to use latest sensors available without changing other software
  - Reuse sensor interfaces, processing components and ICU hardware



Mission-specific sensor suite with standard components

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Hi-Res Camera
GBit

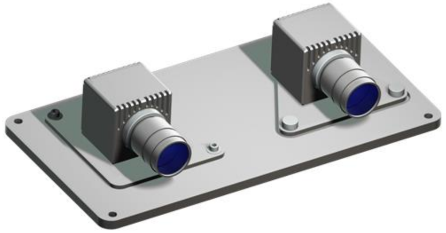
TIR Camera
Gbit

ToF Camera
GBit

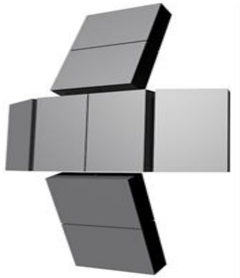
COTS Hi-Res Camera
GBit

WA Illumination
Trigger & RS232

Pattern Projector
Trigger



Stereo Camera
GBit

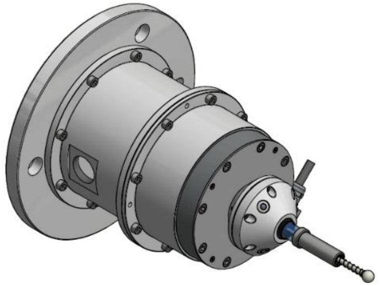


Radar
SpW

LIDAR
Gbit & RS232

IMU
RS485

Star Tracker
SpW



Tactile & Torque
LVDS

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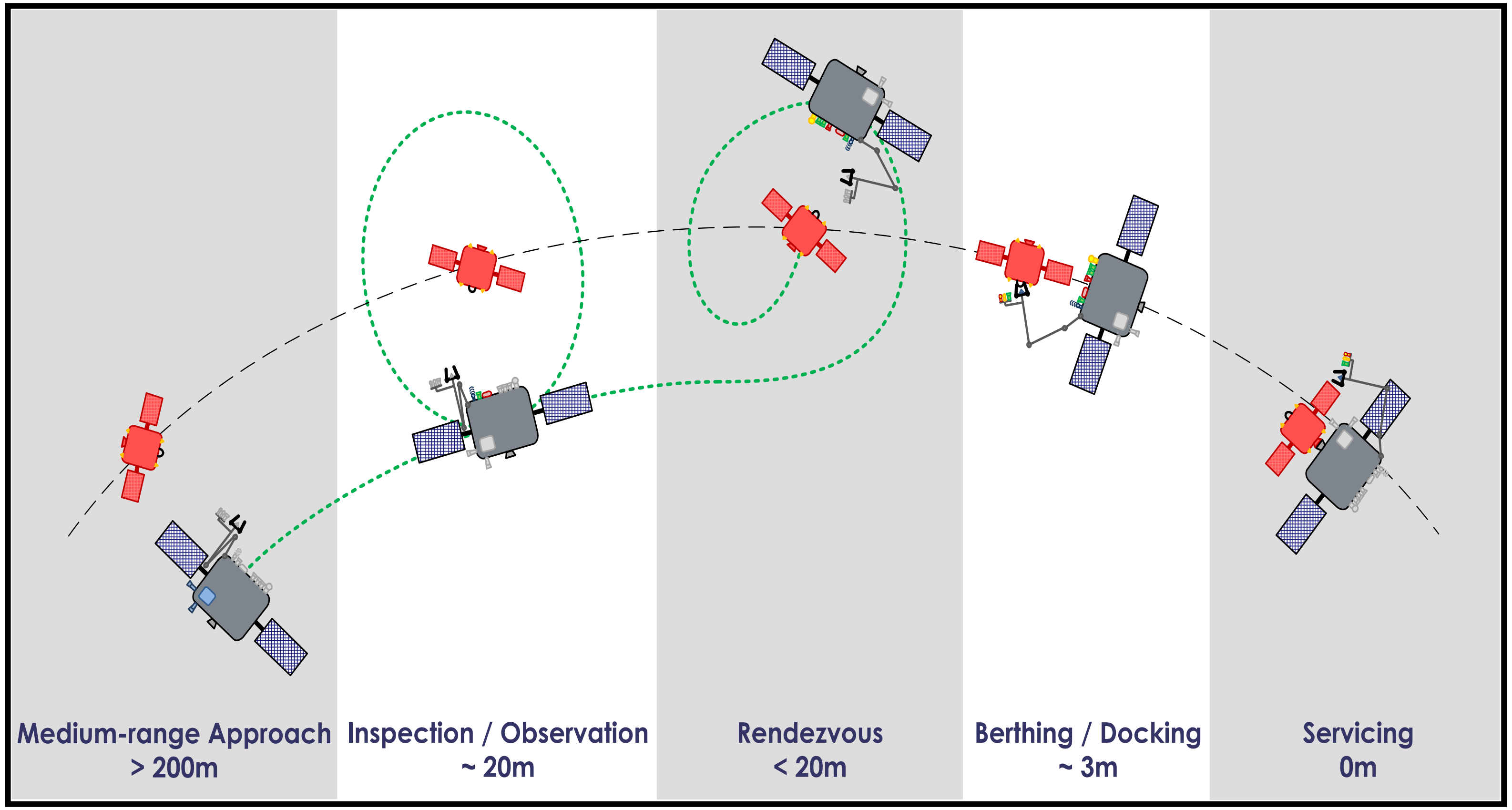
Demonstrator with orbital use-case



TAS-F in Cannes

Demonstrator for planetary use-case

TAS-I in
Torino

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Lab-bench at SINTEF

- Integration of sensors with ICU and testing of functionality and real-time properties
- Recording of coherent data from all sensors moving on trolley
- Sent for mechanical integration at PIAP this week (June 2018)

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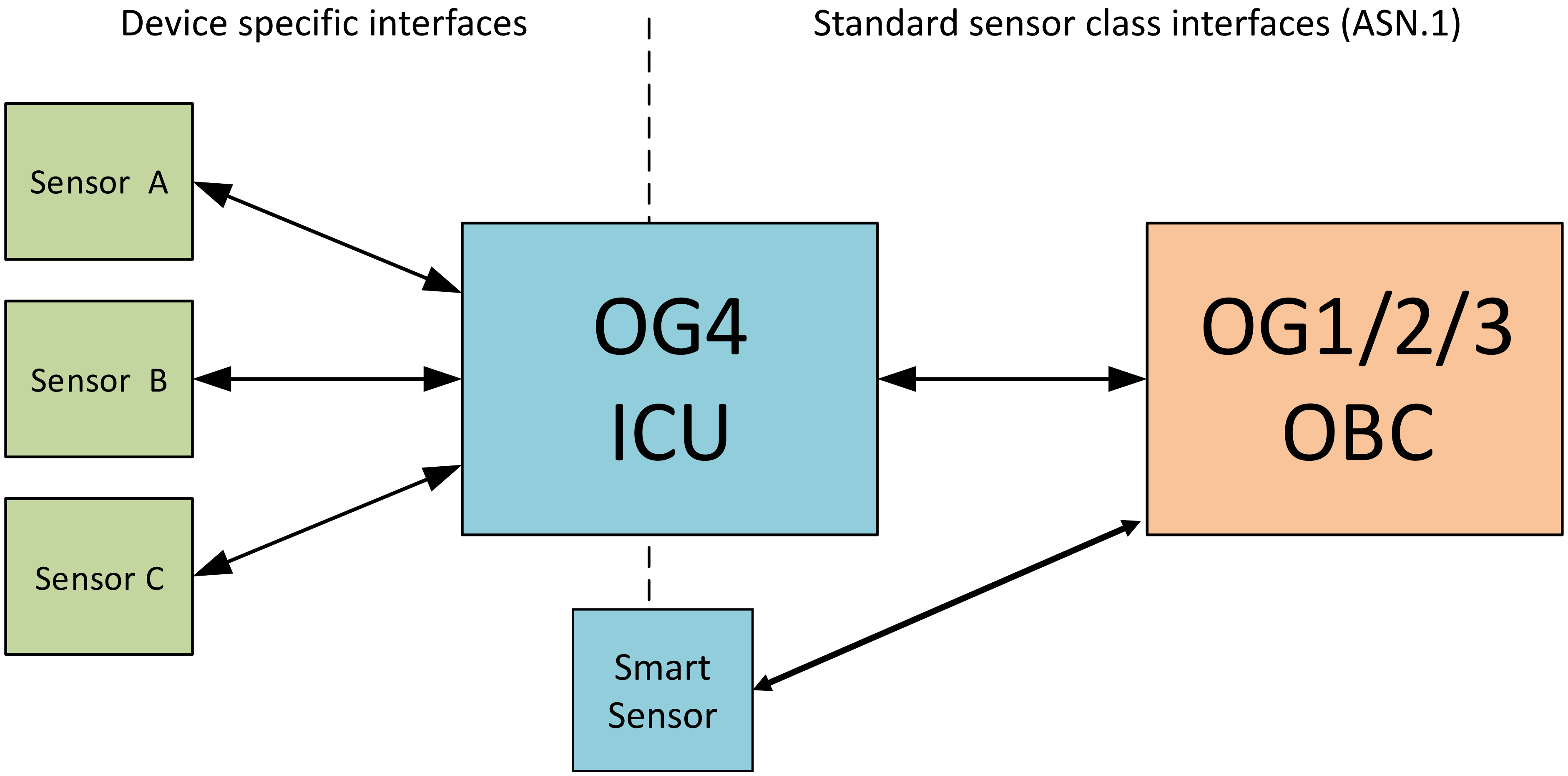
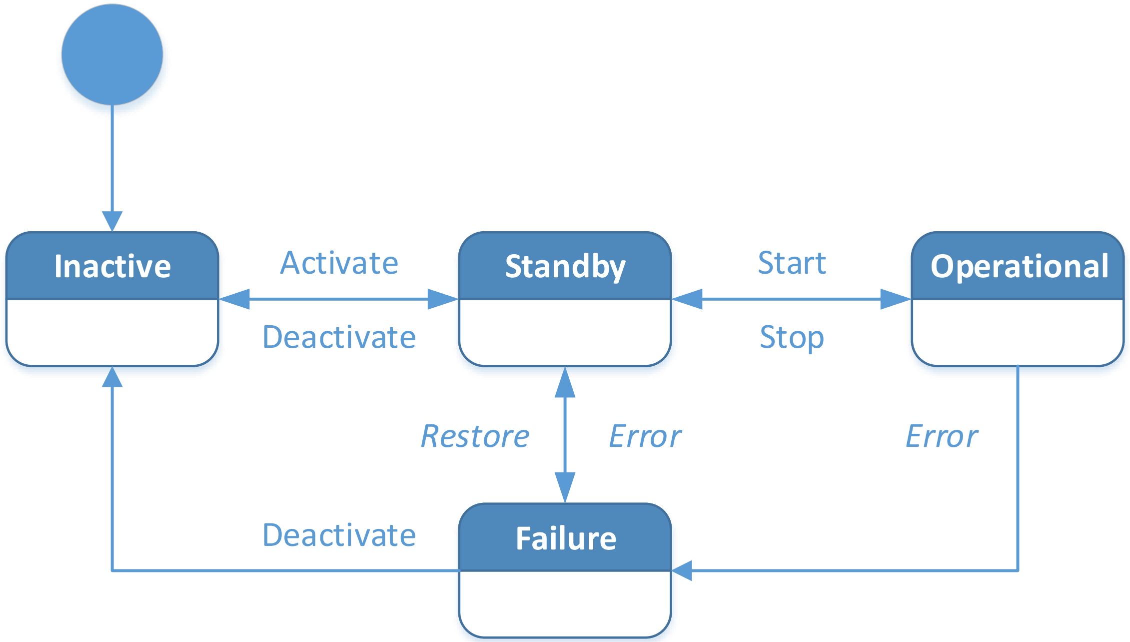
Software architecture



Sensor interfaces



- Common ASN.1 commands and queries
  - State changes inactive ↔ standby ↔ operational
  - Set sample rate and sample batch size of sensor
  - Get configuration, state and temperature of sensor
- Each *sensor class* has its own message interface definitions
  - Camera, ToF camera, LIDAR, radar, star tracker, IMU, analogue sensors
  - Class specific commands, queries and measurements
  - Implemented by concrete sensor drivers and emulator
- Example: Camera class with shutter time, gain, flash, image frames…

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ASN.1 compiler

- Use ASN1CC in project
  - Same as used in TASTE framework
  - Coded in F# and running on mono
  - Outputs code in C and Ada/SPARK
  - SPARK allows for formal verification
  - Currently use C version due to issues in Ada implementation
- uPER encoding for standard messages
- Devices interfaces with ACN

https://github.com/ttsiodras/asn1scc

```
DMU30-Types DEFINITIONS ::= BEGIN

    Word-Type[size 16, encoding pos-int]
    Real-Type[encoding IEEE754-1985-32]

    …

    Message-Type[]
    {
       header NULL [pattern '0101010110101010'B],
       message-count[],
       axis-x-rate[],
       axis-x-acceleration[],
       axis-y-rate[],
       axis-y-acceleration[],
       axis-z-rate[],
       axis-z-acceleration[],
       aux-input-voltage[],
       average-temperature[],
       axis-x-delta-theta[],
       axis-x-vel[],
       axis-y-delta-theta[],
       axis-y-vel[],
       axis-z-delta-theta[],
       axis-z-vel[],
       startup-flags[],
       operation-flags[],
       error-flags[],
       checksum NULL [pattern '0000000000000000'B]
    }

END
```

Computation and throughput load

*absolute best case

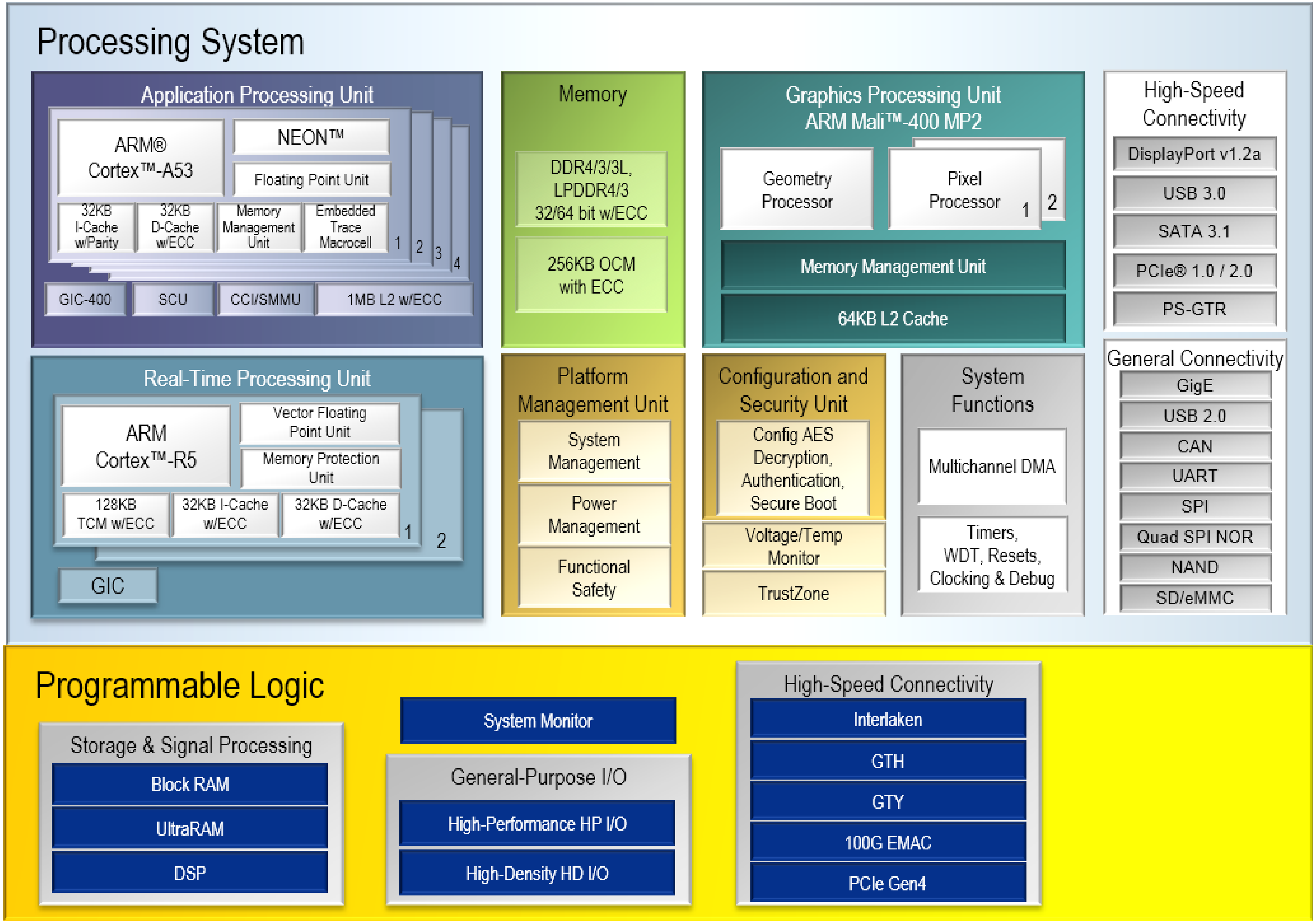
Sensor	Sample size	Rate	Throughput*
HR camera	2048*2048*2 Bytes = 8 MiB	10 Hz	84 Mb/s
Stereo camera	2*2048*2048*2 Bytes = 16 MiB	10 Hz	168 Mb/s
ToF camera	640*480*5 Bytes = 1500 KiB	10 Hz	15 Mb/s

- Lens distortion correction
- Histogram equalization
- CLAHE
- Bilateral filtering
- Stereo rectification
- Point-cloud generation

Instrument Control Unit

- ICU build on the Xilinx Zynq UltraScale+ MPSoC
  - Mixed-criticality real-time system
  - Quad-core ARM Cortex A53 with Xilinx PetaLinux
  - Two ARM Cortex R5 real-time processors
  - FPGA for bespoke hardware modules
  - ARM Mail GPU for processing with support for OpenCV
- Runs sensors interfaces and pre-processing algorithms
- **The Xilinx Zynq UltraScale+ is a complex platform!**

Avnet UltraZED-EG SOM


Processing System
Application Processing Unit
ARM® Cortex™-A53
NEON™
Floating Point Unit
32KB I-Cache w/Parity
32KB D-Cache w/ECC
Memory Management Unit
Embedded Trace Macrocell
1
2
3
4
GIC-400
SCU
CCI/SMMU
1MB L2 w/ECC
Memory
DDR4/3/3L, LPDDR4/3 32/64 bit w/ECC
256KB OCM with ECC
Graphics Processing Unit ARM Mali™-400 MP2
Geometry Processor
Pixel Processor
1
2
Memory Management Unit
64KB L2 Cache
High-Speed Connectivity
DisplayPort v1.2a
USB 3.0
SATA 3.1
PCIe® 1.0 / 2.0
PS-GTR
Real-Time Processing Unit
ARM Cortex™-R5
Vector Floating Point Unit
Memory Protection Unit
128KB TCM w/ECC
32KB I-Cache w/ECC
32KB D-Cache w/ECC
1
2
GIC
Platform Management Unit
System Management
Power Management
Functional Safety
Configuration and Security Unit
Config AES Decryption, Authentication, Secure Boot
Voltage/Temp Monitor
TrustZone
System Functions
Multichannel DMA
Timers, WDT, Resets, Clocking & Debug
General Connectivity
GigE
USB 2.0
CAN
UART
SPI
Quad SPI NOR
NAND
SD/eMMC
Programmable Logic
Storage & Signal Processing
Block RAM
UltraRAM
DSP
System Monitor
General-Purpose I/O
High-Performance HP I/O
High-Density HD I/O
High-Speed Connectivity
Interlaken
GTH
GTY
100G EMAC
PCIe Gen4

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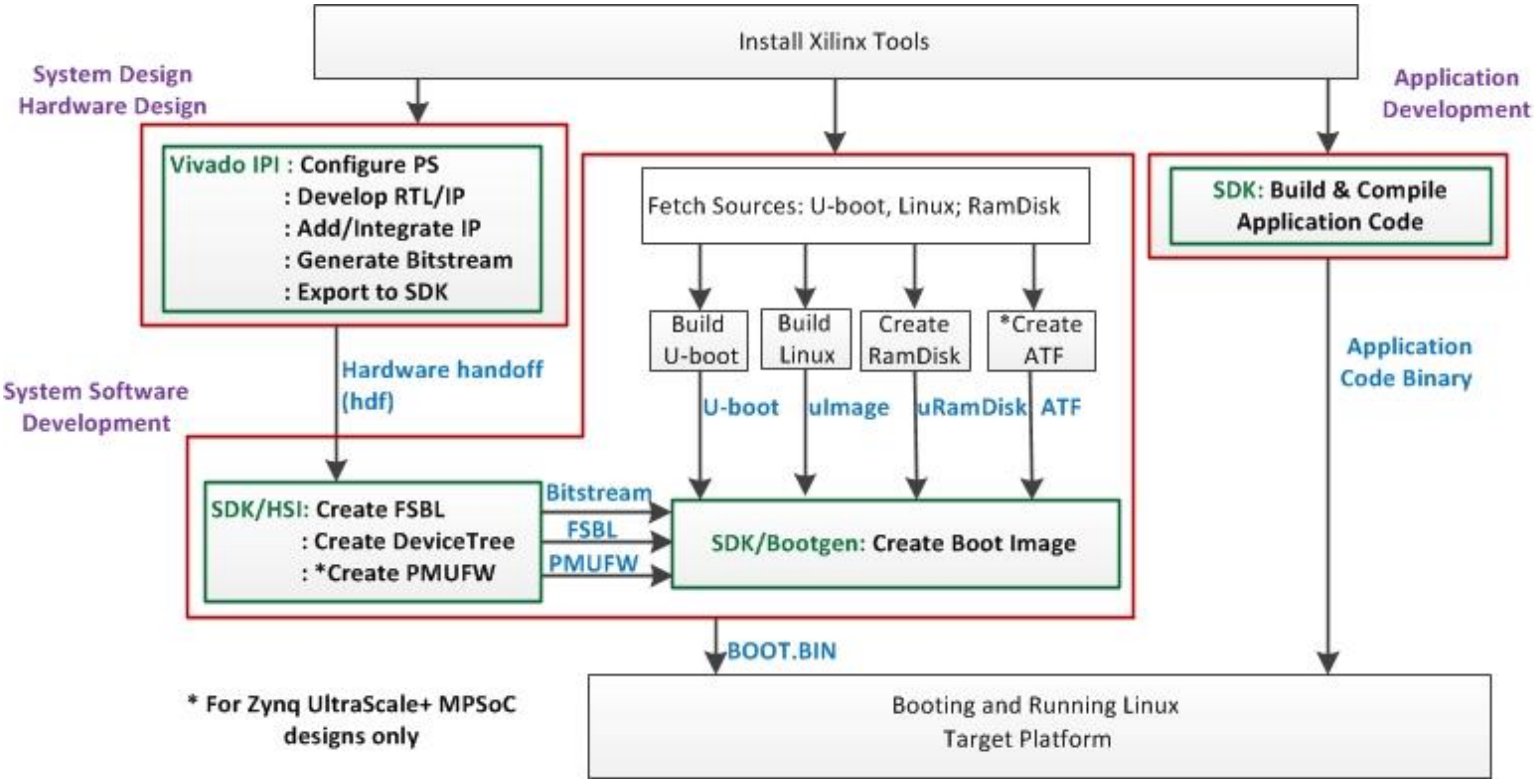
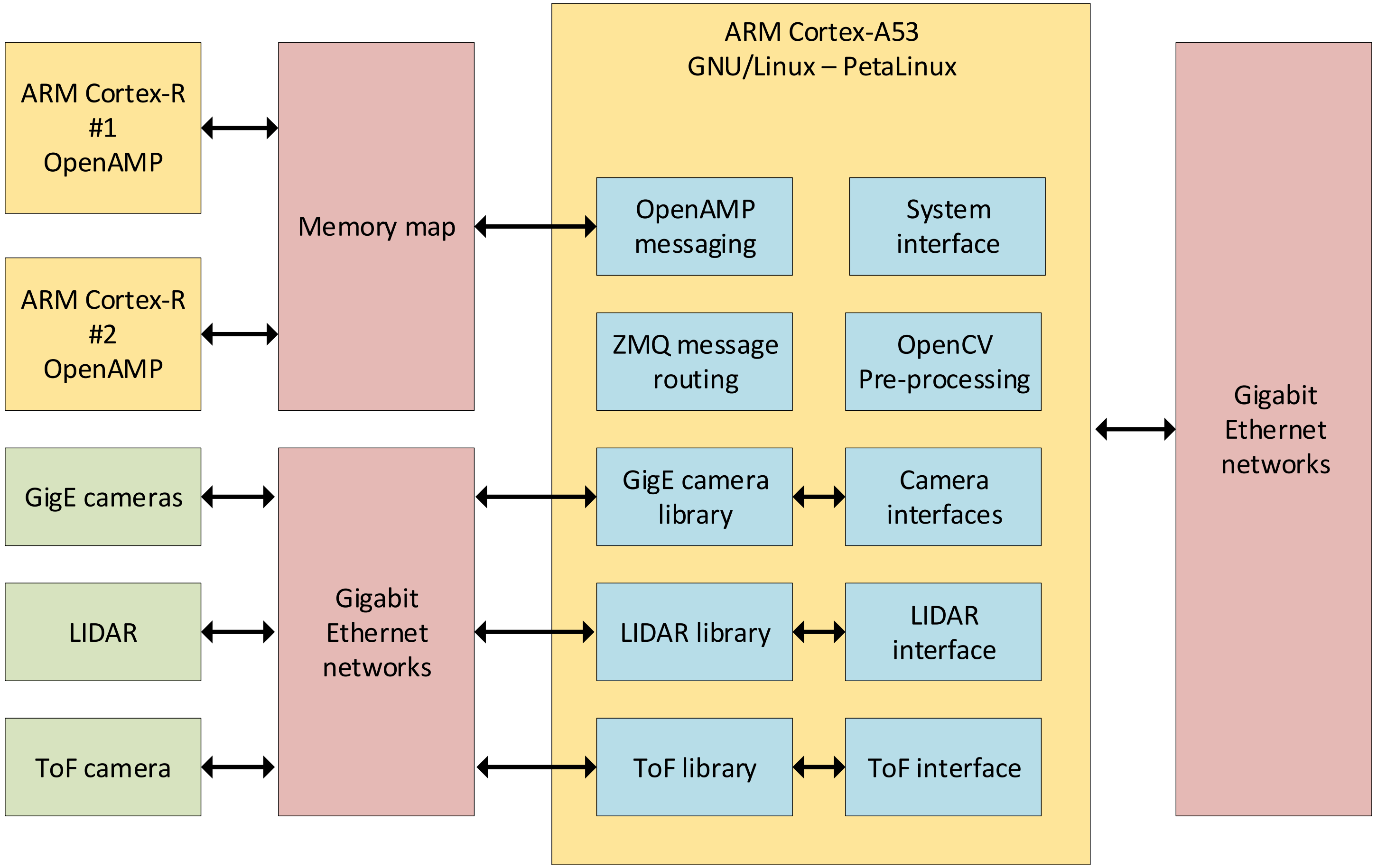

Install Xilinx Tools
System Design
Hardware Design
Application
Development
Vivado IPI : Configure PS
: Develop RTL/IP
: Add/Integrate IP
: Generate Bitstream
: Export to SDK
Fetch Sources: U-boot, Linux; RamDisk
SDK: Build & Compile
Application Code
Build
U-boot
Build
Linux
Create
RamDisk
*Create
ATF
Hardware handoff
(hdf)
System Software
Development
U-boot
uImage
uRamDisk
ATF
Application
Code Binary
SDK/HSI: Create FSBL
: Create DeviceTree
: *Create PMUFW
Bitstream
FSBL
PMUFW
SDK/Bootgen: Create Boot Image
BOOT.BIN
* For Zynq UltraScale+ MPSoC
designs only
Booting and Running Linux
Target Platform

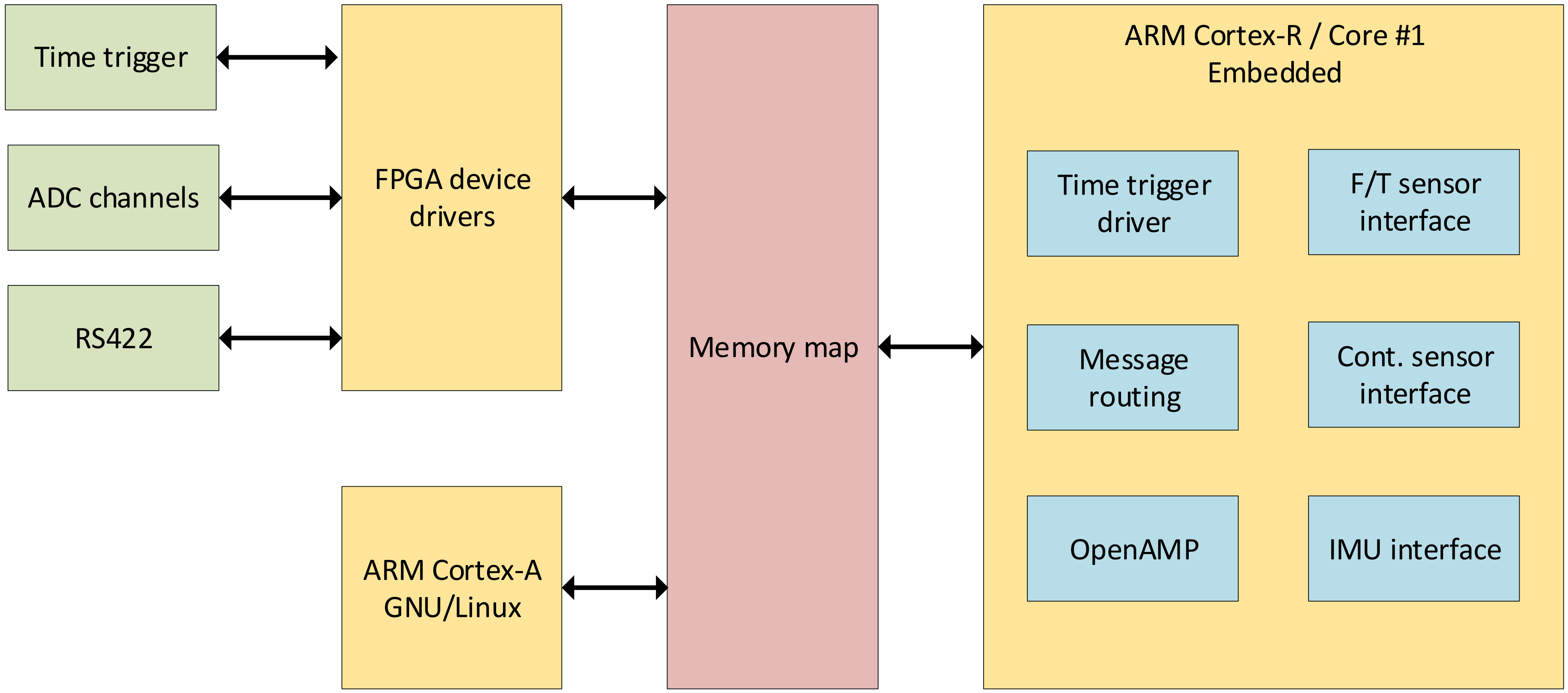
ICU mixed criticality real-time system

- Xilinx PetaLinux on Cortex A53
  - Interfaces to GigE vision cameras and COTS sensors
  - System interface to OG1/2/3 over GigaBit Ethernet
  - Use ZMQ library for high-performance messaging over TCP/IP
  - C++ framework developed for sensor interfaces, clients and emulators
  - OpenCV used for image processing, e.g. stereo image to point-cloud
- Embedded and real-time software on Cortex R5
  - ADC polling for tactile and F/T sensors, IMU, triggers, and SpW interfaces…
  - Ada/SPARK used for sensor control and processing
- Communicate in memory-buffers between cores using OpenAMP

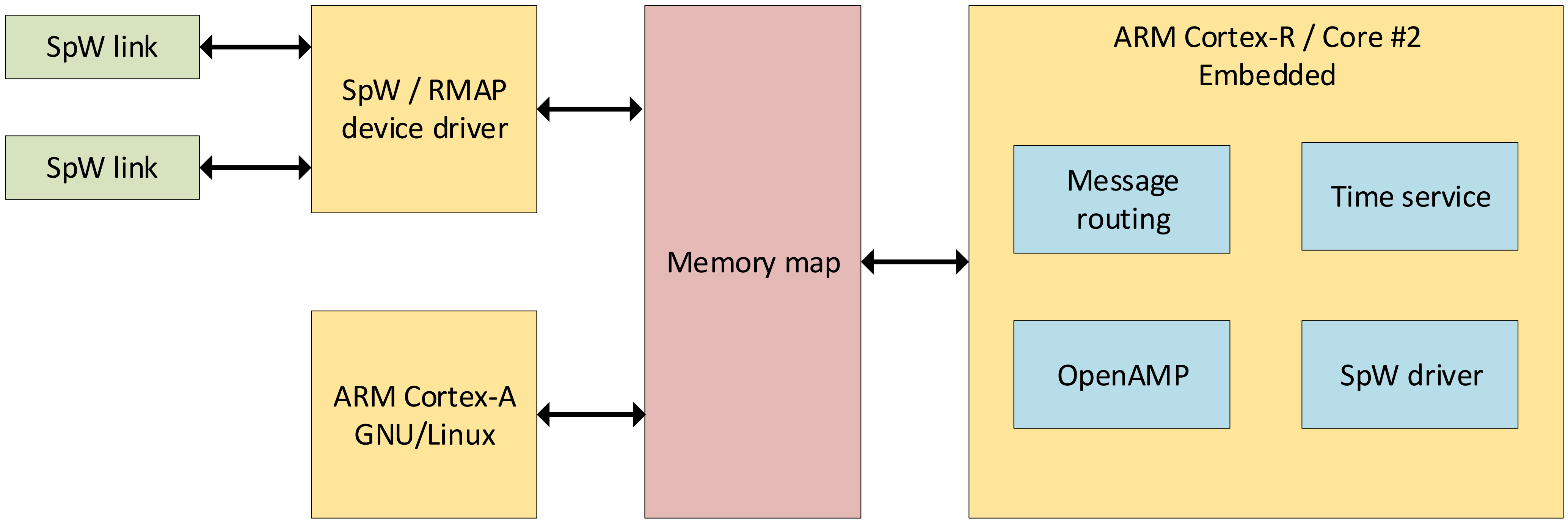
Cortex A53 with Xilinx PetaLinux



Cortex R5 #1 with device interfaces



Cortex R5 #2 with SpaceWire interface



Ada and SPARK 2014 on the Cortex R5

- Use GNAT Pro Developer for ARM with SPARK 2014 tools
  - No Ravenscar run-time for the Zynq UltraScale+ MPSoC
  - Adapted zero footprint (ZFP) run-time from TMS570 (Cortex R4/5)
  - GNAT Pro makes it very easy to reconfigure and recompile run-times
- Develop static library with functionality in Ada/SPARK 2014
- Xilinx SDK for FreeRTOS, device interfaces, linking and programming
- Match ABI and compile flags for GNAT and Xilinx SDK (both use GCC)

Functionality made in SPARK 2014

- Interfaces for IMU and ADC sensors
  - Sensor state machines and command handling
  - Process, accumulate, and send sensor measurement data
  - IMU needs temperature-dependent correction with calibration data
  - ADC readings are converted to physical floating-point value
  - Hard real-time demands, sampling at 200 Hz and 1000 Hz
- Formal proof of correctness for sensor state machine
- Flow control and dependencies for data processing
- SPARK 2014 allows us to develop code with confidence!

Forward to a certifiable software system

- All critical functionality and Space Wire/Fibre on Cortex R5 and FPGA
- Want to have certified Ravenscar run-time on the Cortex R5
  - Need to integrate GNAT Pro with Xilinx SDK or the other way around? Reuse drivers?
  - Bonus: FPGA gives great opportunities for specialized support hardware (e.g. TMU)
- Mixed-criticality with the Cortex A53 and PetaLinux
  - Xilinx reVISION provides FPGA-accelerated OpenCV and more
  - PetaLinux with accelerated OpenCV for heavy camera pre-processing
  - Could use hypervisor such as XtratuM for improved isolation
- Coming GNAT for ARM64 allows use on PetaLinux too!

Conclusions

- Future robotics applications require high-performance computer platforms for AI, image processing, machine learning etc.
- The Xilinx UltraScale+ MPSoC with accelerated OpenCV and real-time functionality with Ravenscar and SPARK 2014 is very promising!
- Need good integration between Xilinx tools generating hardware, PetaLinux, hypervisor, and GNAT Pro for safety-critical real-time code
- We want to use this mixed-criticality real-time system and SPARK for our autonomous robots and high-performance edge computing!

H2020 Space Robotic SRC- OG4

INTEGRATED 3D SENSORS

« Smart Sensors for Smart Missions »

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 730118

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Technology for a better society